

Examiner's Amendment

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2. (Currently Amended) The method as claimed in claim 1, characterized in that provision is made of corresponding devices (4, 8; 5, 10; 7, 12) for compensation of the interference ~~both in the time domain and in the frequency domain.~~

3. (Currently Amended) The method as claimed in claim 1, characterized in that coefficients which are calculated from ~~[[the]]~~ an error-corrected digitized samples are fed to a system analysis unit (6) from which the properties of the transmission channel are calculated.

4. (Currently Amended) A circuit arrangement for carrying out the method as claimed in claim 1, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal are ~~providable can be fed~~;

at least one subtractor circuit (16), each subtractor circuit (16) calculating a difference between ~~subtracting~~ a digitized sample of the symbol ~~[[from]]~~ and a digitized sample assigned thereto of the cyclic prefix preceding the symbol for a calculation of ~~[[the]]~~ an error on account of the transient process; and

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, the at least one multiplier circuit (17, 18) being assigned to each digitized sample of ~~[[a]]~~ the symbol;

~~it being possible for~~ wherein the output signal of each subtractor circuit (16) ~~to be fed~~ is providable in each case to each multiplier circuit (17, 18); and